Semiconductor Electronics: Materials, Devices and Simple Circuits

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Any device whose action is based on the controlled flow of electrons through it is called an electronic device.

The branch of physics that deals with the study of these electronic devices is called electronics.

Energy Band

Formed due to the interaction of electrons with neighbouring atoms.

(i) First energy band
energy possessed by all first orbit electronics

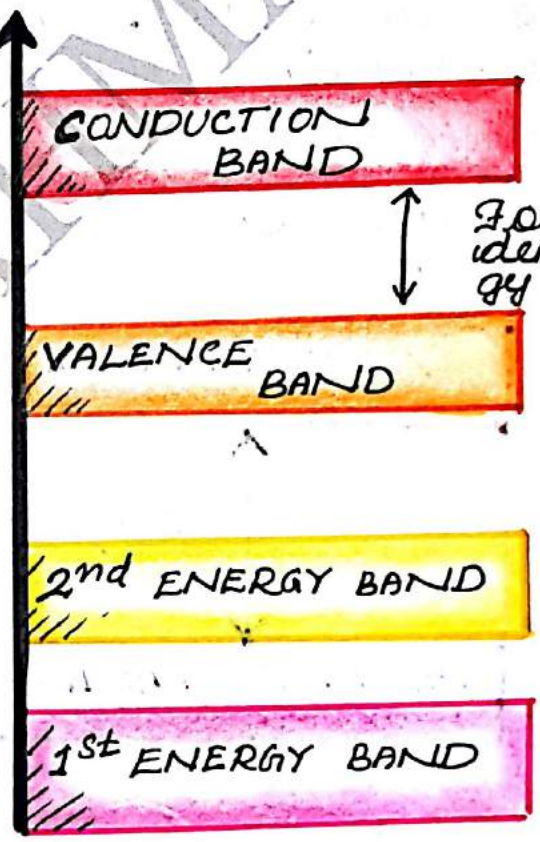
(ii) second energy band.
energy possessed by second orbit electrons.

(iii) Valence band
energy possessed by valence electrons.

(iv) conduction band.
energy possessed by free electrons

(v) Forbidden energy gap [Eg].
energy gap between valence and conduction bands.
for Si → Eg = 1.21eV at 0K
for Ge → Eg = 0.785 eV "

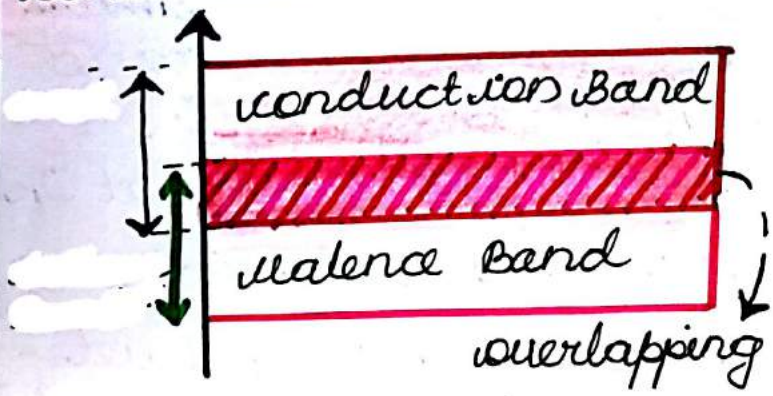
(vi) Fermi energy level -
The highest energy level an electron can occupy in valence band at 0K.



classify solids (conductors Insulators and semiconductors) on the basis of energy band diagram.

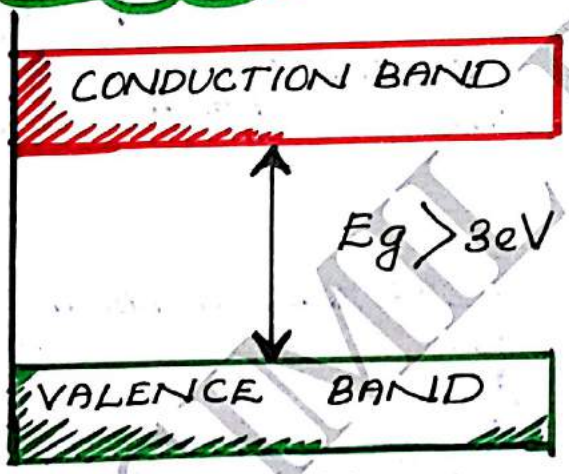
conductors (metals)
valence band overlaps conduction band. Therefore electrons from valence band

can move easily to the conduction band.



→ All ē's in valence band can go to conduction band without any external energy, which is responsible for conduction.

Insulators

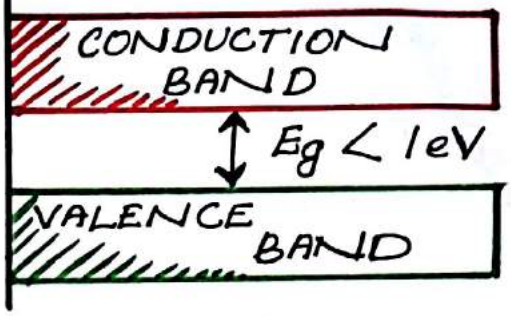


→ large forbidden energy gap between valence band and conduction band ($E_g > 3eV$).

→ electrons can go to conduction band from valence band if large amount of energy is supplied.

→ Thus they behave as insulators.

semiconductors



→ Forbidden energy gap between valence and conduction band is very less

→ Even at room temperature electrons in valence band can escape to conduction band which is responsible for conduction.

Types of Semiconductors

1. Intrinsic semiconductors

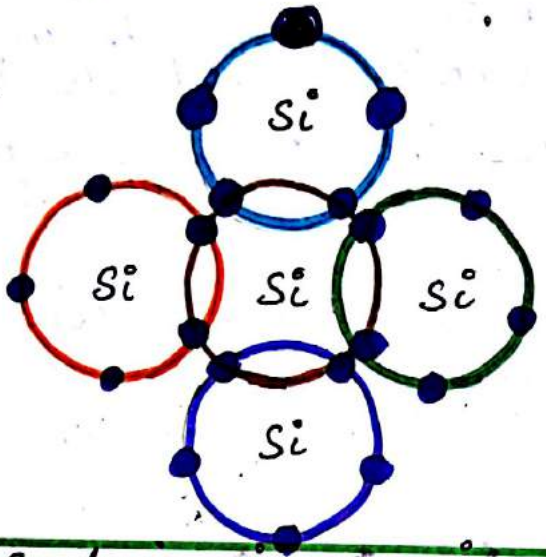
→ purest form of semiconductors

→ No of electron = no of holes

→ Eg: Si, Ge – tetravalent

→ Forms covalent bond with other silicon atoms.

→ only due to thermal agitation one or two electrons escape from covalent bond.



2 Extrinsic Semiconductors.

→ Impure form

Doping – process of adding impurities (penta valent or trivalent) with **Si** or **Ge**

The impurity atoms are called dopands.

The semiconductor containing impurity atoms is known as extrinsic semiconductor.

Types of extrinsic Semiconductors.

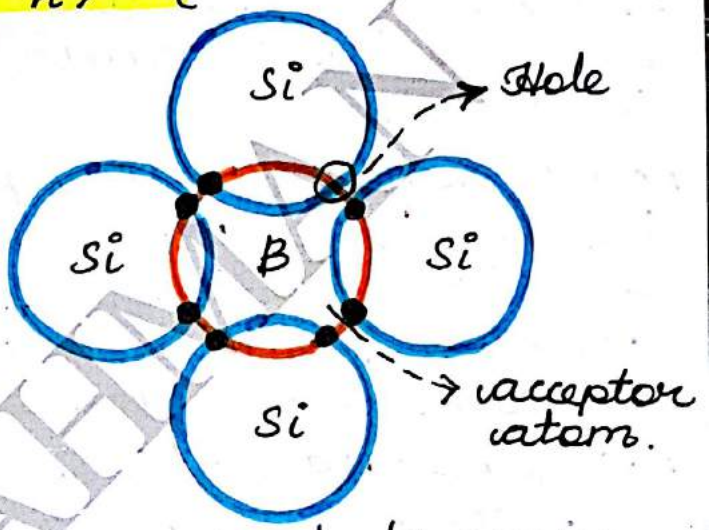
1, P-type Semiconductors.

→ Formed when Si and Ge doped with trivalent impurity.

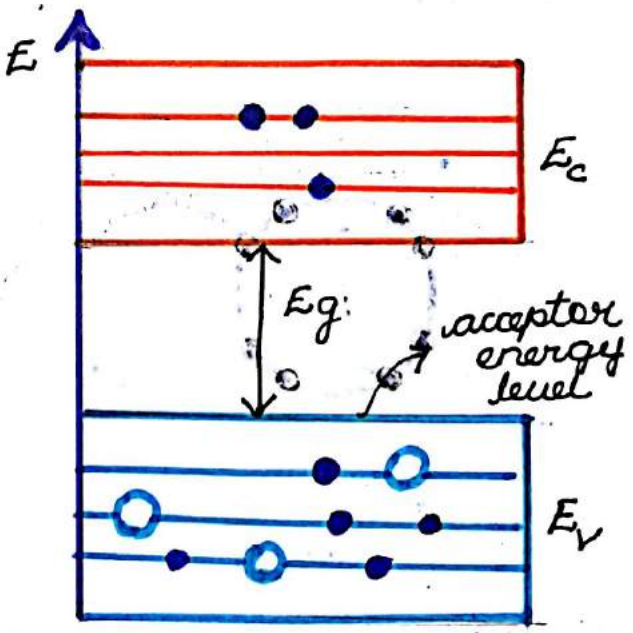
→ all **3** electrons from boron form covalent bond with **Si** atom, leaving a deficiency of 1 electron called hole. that can accept electrons.

→ so trivalent impurity atoms (eg. boron) called acceptor atoms.

→ $n_h > n_e$



Energy Band diagram for p-type Semiconductor.



→ $n_h > n_e$

→ acceptor energy level is just above valence band.

→ Holes are majority carriers and electrons are minority carriers.

→ electrons due to thermal agitation.

→ Holes due to doping and thermal agitation

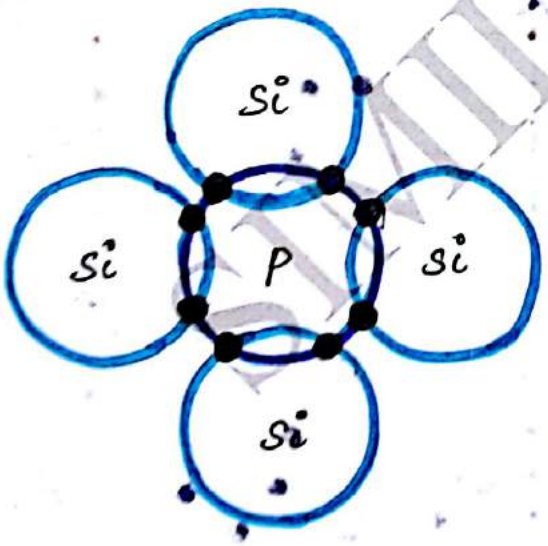
N-type Semiconductors.

→ Formed when 'Si' or 'Ge' doped with pentavalent impurity.

→ each pentavalent impurity forms covalent bond with Si atom and donates 1 electron to the semiconductor.

→ so pentavalent impurity atom (eg- phosphorous) called donar atom.

→ $n_e > n_h$

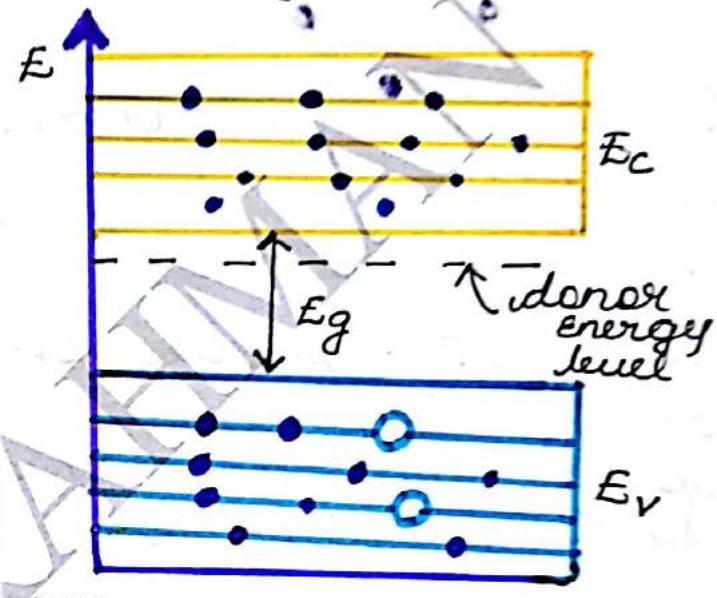


Energy Band diagram for n-type Semiconductor

→ $n_e > n_h$

→ Donar energy level is just below conduction band.

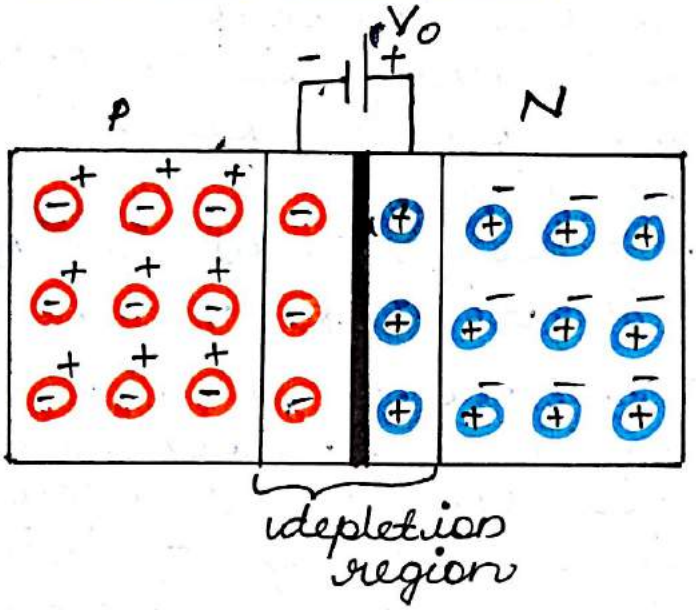
* electrons in conduction band is due to thermal agitation and doping.
* Holes in valence band due to thermal agitation.
* electrons are majority carriers and holes are minority carriers.



Differentiate N-type and P-type Semiconductors.

N-type	P-type
1, Formed when Si or Ge doped with pentavalent impurity eg, Phosphorous	1. Formed when 'Si' or 'Ge' doped with trivalent impurity eg, Boron.
2. electrons are majority carriers.	2, Holes are majority carriers.
3, Holes are minority carriers.	3, Electrons are minority carriers.
4, $n_e >> n_h$	4, $n_h >> n_e$

Explain the formation of PN - Junction diode. depletion region and barrier potential.



⊖ Immovable acceptor atom

⊕ Immovable donar atom.

\+ movable hole

− movable electron.

* Dope one side of 'Si' wafer with trivalent and other portion with pentavalent impurity - forms pn junction diode.

* P type semiconductor has immovable acceptor atom ⊖ and movable hole +

* N type semiconductor has immovable donar atom ⊕ and movable electrons −

Diffusion

③

At the junction diffusion takes place, electrons and holes cross the junction get neutralised, leaving immovable acceptor ions ⊖ and donar ions ⊕ at the junction.

Depletion region

region which has immobile donar and acceptor ions of width 10^{-4} cm to 10^{-6} cm called depletion region

Internal potential barrier (V_o)

The potential difference across the depletion region due to immobile donar and acceptor ions.

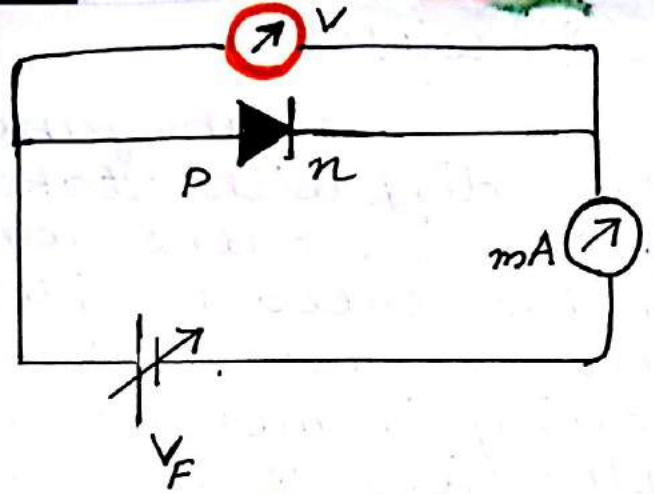
for Si → IPB is 0.7V at 25°C

for Ge → IPB is 0.3V at 25°C

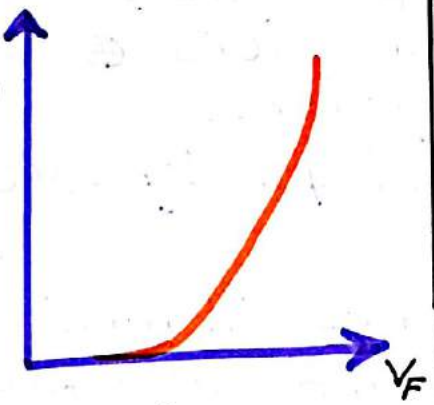
* Explain with the help of a circuit diagram how V-I characteristics of a PN-junction diode are obtained in

(i) Forward bias

(ii) Reverse bias.

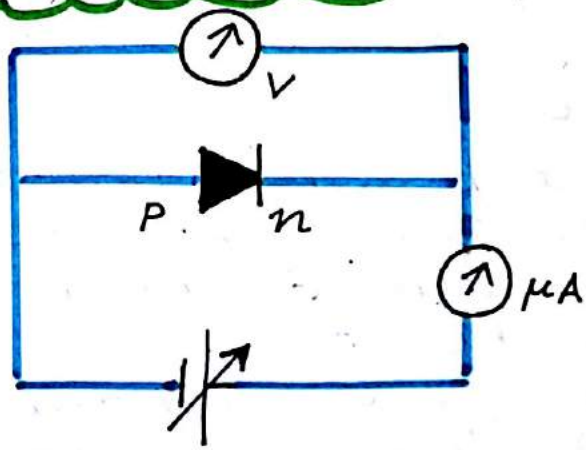


V-I characteristics in forward bias



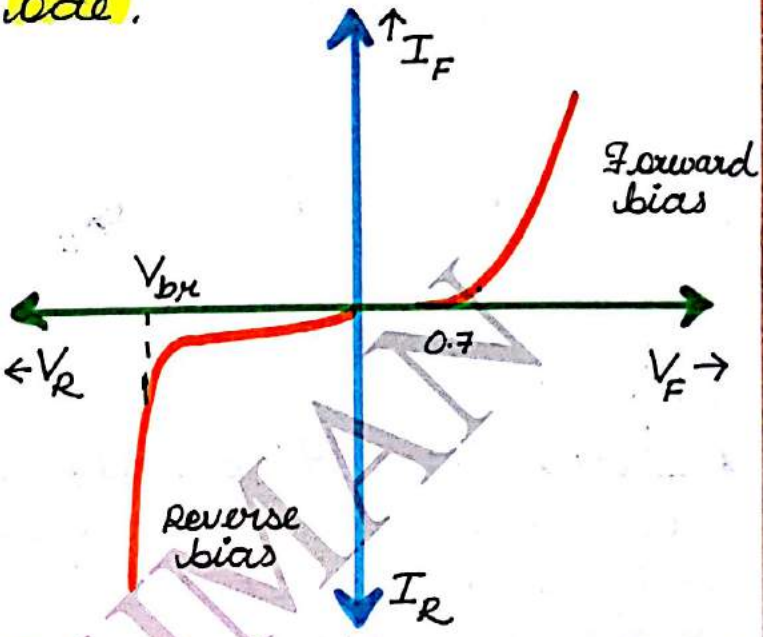
* In forward bias, p-type semiconductor is connected to '+'ve and n-type semiconductor is connected to '-'ve terminal.
* Increase forward voltage V_F.
* If $V_F < V_0$ majority carriers cannot cross the junction $I_f = 0$
* still increase V_F, when $V_F > V_0$, I_f increases due to majority carriers.
* In forward biasing the current is due to majority carriers.
* when majority carriers cross the junction, the width of depletion region decreases and vanishes. potential barrier voltage also reduced.
* Holes in the P-region and electrons in the N-region can flow across the junction without any resistance offered by the potential barrier.
* It result in an exponential rise in current.
* The potential V_F at which this exponential rise of current occures is called offset, firing or threshold voltage. $V_T = 0.7V$ for Si & Ge $V_T = 0.3V$.
* The reason for this cumulative effect is when $V_F \uparrow$ speed of electrons and holes increases, knocks out electrons from co-valent bond, e-hole pair created, $\therefore I_F \uparrow$, Heat $\uparrow$, Temp $\uparrow$.

Reverse Bias.



* Diode offers high resistance in the reverse bias condition.
* In reverse bias p-type semiconductor is connected to '-'ve terminal and n-type is connected to '+'ve terminal.
* Due to reverse bias, majority carriers are moving away from the depletion region.
* But minority carriers cross the junction.
* It is also called as instrinsic current
* So current in the diode is due to minority carriers (very less)
* If $V_R \uparrow$ $I_R \uparrow$
* Still increase of V_R, collision increases, breaks covalent bond - produces electron hole pair Due to collision it breaks many covalent bonds - avalanche effect is produced. This cumulative phenomenon is called avalanche breakdown.
* At this particular voltage (break down voltage) current increases enormously.
* An Ideal diode does not conduct in reverse bias.

V-I characteristic curve for PN junction diode.



Application of PN-junction diode - Rectifier.

What is meant by Rectification?

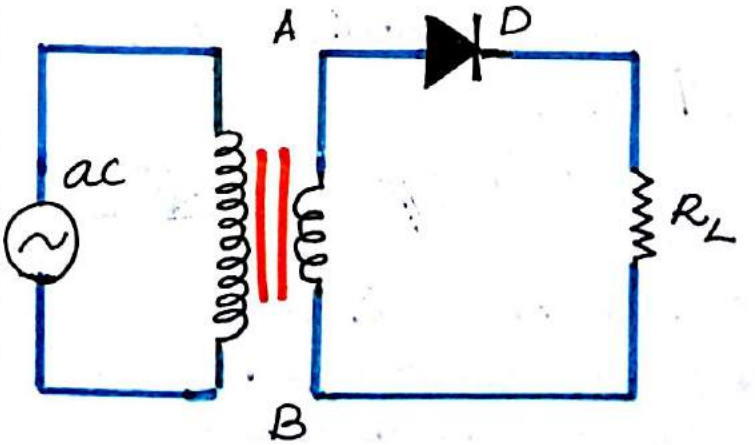
Rectification

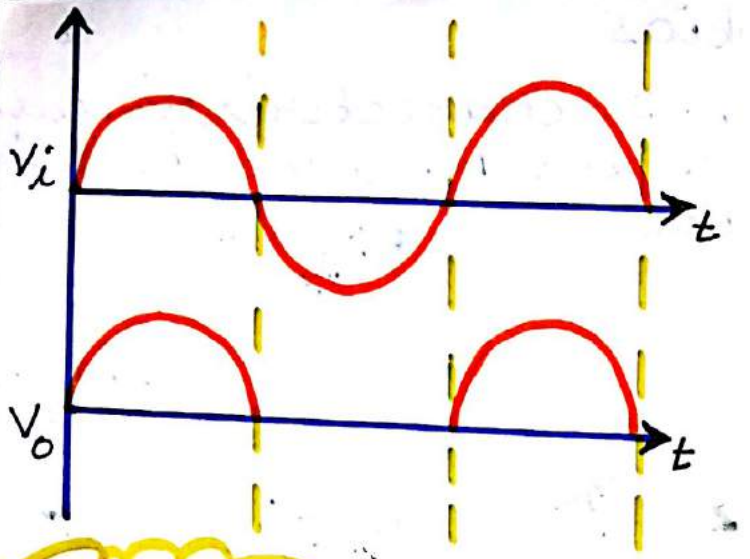
Means conversion of ac into dc.

Rectifier

Electronic Device which converts ac into dc.

Half Wave Rectifier.





principle

* Junction diode offers low resistance for forward bias and high resistance for reverse bias.
* Diode conducts when forward biased and does not conduct when reverse biased.

Arrangement.

* Ac to be rectified is applied to the primary of transformer.
* secondary of transformer is connected to the diode D and load resistance R_L.
* output voltage is obtained across R_L.

Theory

During +ve half cycle.

* A is '+ve' w.r.t B.
* Diode conducts as it is forward biased.
* Potential is dropped across R_L.

During -ve half cycle

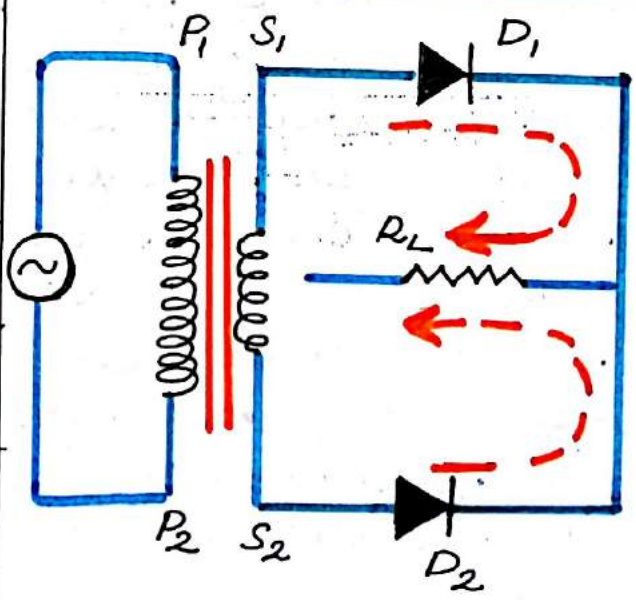
* A is '-ve' with. r.t B.
* Diode does not conduct as it is reverse biased.

Thus the Diode D changes ac into dc, the output is unidirectional.

only half of the input ac is rectified. so it is called half wave rectifier.

note:- The effeciency is 40.6%.

Full Wave Rectifier



Principle

Junction diode conducts when it is forward baised and

does not conduct when reverse biased.

Arrangement.

→ Ac to be rectified is applied to primary transformer

→ secondary is connected to D_1 and D_2 and a load resistance R_L to centre tap O.

Theory

1, During positive Half cycle.

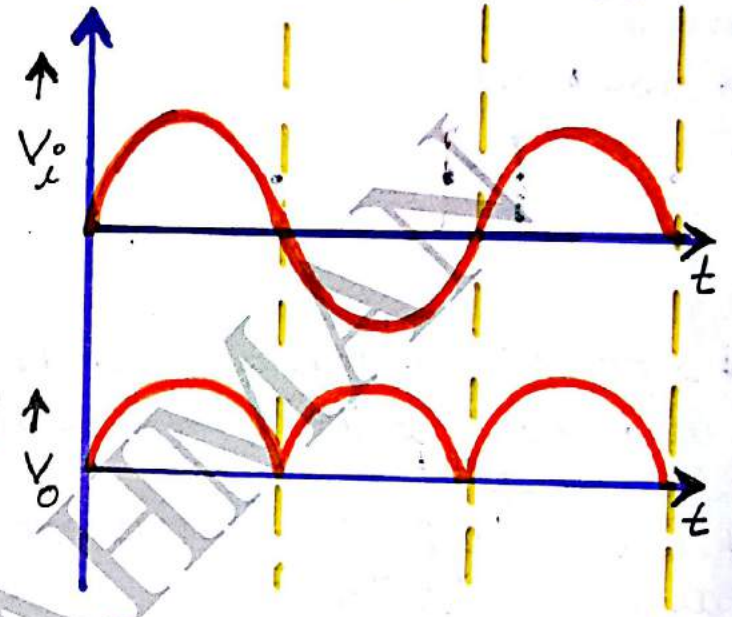
* S_1 is +ve with respect to O
* S_2 is -ve w.r.t O.
* D_1 conducts as it is forward biased, from right to left through R_L.
* D_2 does not conduct as it is reverse biased.

2, During negative Half cycle.

* S_1 is '-ve' w.r.t O and S_2 is '+ve' w.r.t O
* D_2 conducts as it is forward biased, from right to left through R_L
* D_1 does not conduct as it is reverse biased.

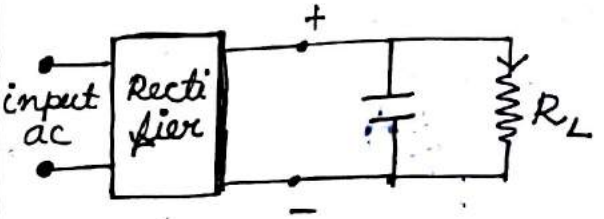
Thus both '+'ve and '-'ve half cycles are rectified ⑤ - called full wave rectifier.

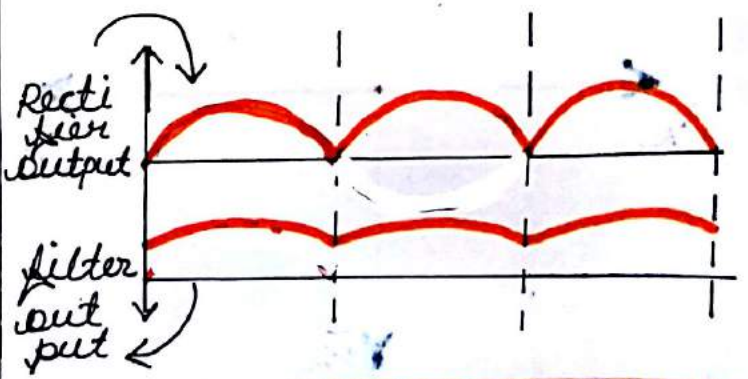
* It is unidirectional
* Efficiency is 81.2%.



Filters

* The output obtained from a junction diode rectifier is unidirectional but pulsating.
* The filters filters out the ac ripple and gives a pure dc voltage.





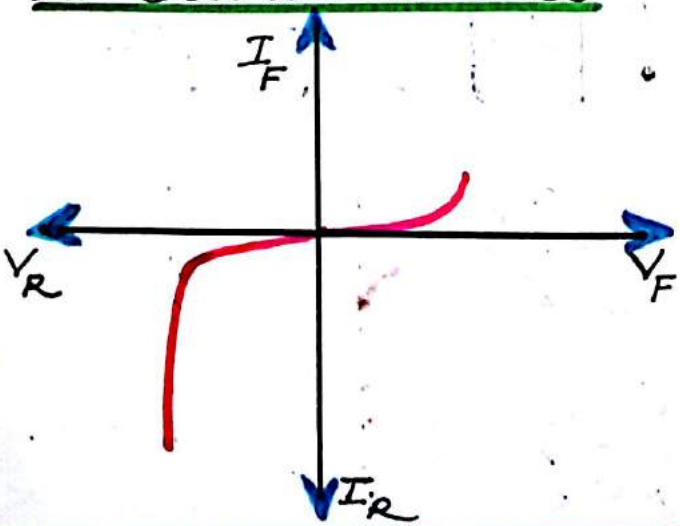
Filters
- series inductor filter
- shunt capacitor filter.

Zenor Diode

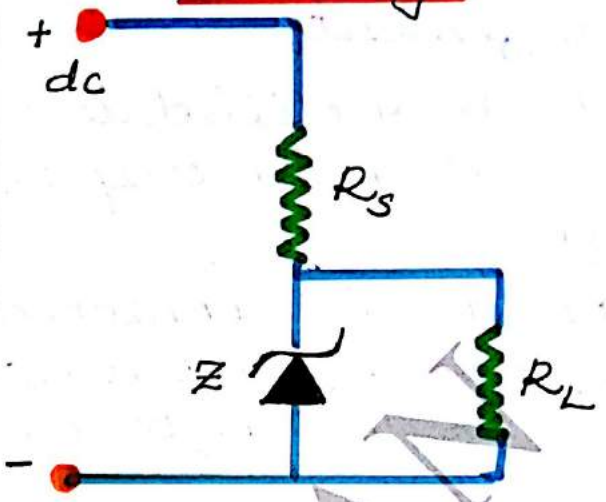
* symbol

* Both p and n sides of a zenor diode is heavily doped
* width of depletion region $\angle 10^{-6}$ m.
* Electric field of the junction is very high (-5×10^{6} V/m)
* Zenor diode is operated in reverse bias - break down region.
* At the break down voltage V_z, for large variation of I, there is an insignificant variation in voltage.

VI characteristics



Voltage regulator - working



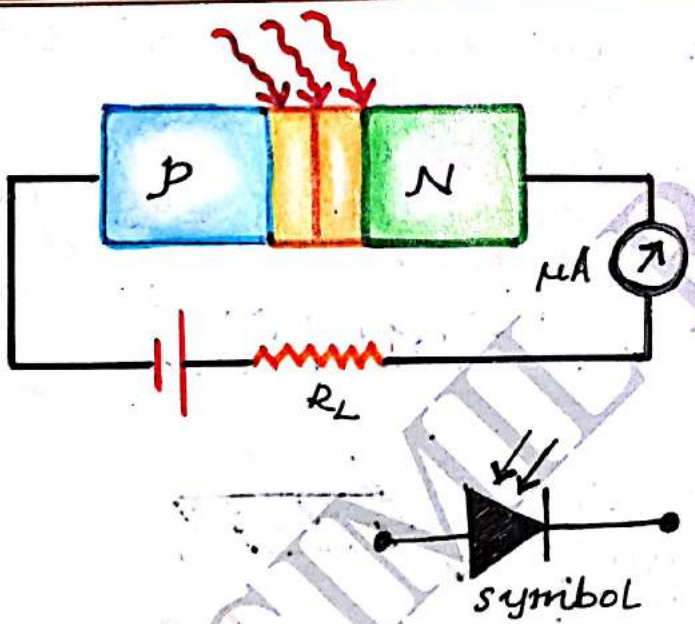
* The unregulated dc voltage from the rectifier is connected zenor diode (D) through a series Resistance (R_S)
* R_L is connected across zenor diode where regulated voltage is collected.
* when dc current ↑ I_{R_S} ↑ , I_z ↑
* as I_{R_S} ↑ V_{R_S} ↑ without changing the zenor voltage V_z - constant
* If DC current decreases ↓, I_{R_S} ↓ and I_z ↓
* as I_{R_S} ↓, V_{R_S} ↓ without changing the zenor voltage V_z - constant.
* Reason :- For a large variation of current voltage remains same in the reverse bias region.

The voltage across R_L remains constant

* Hence zener diode acts as voltage regulator

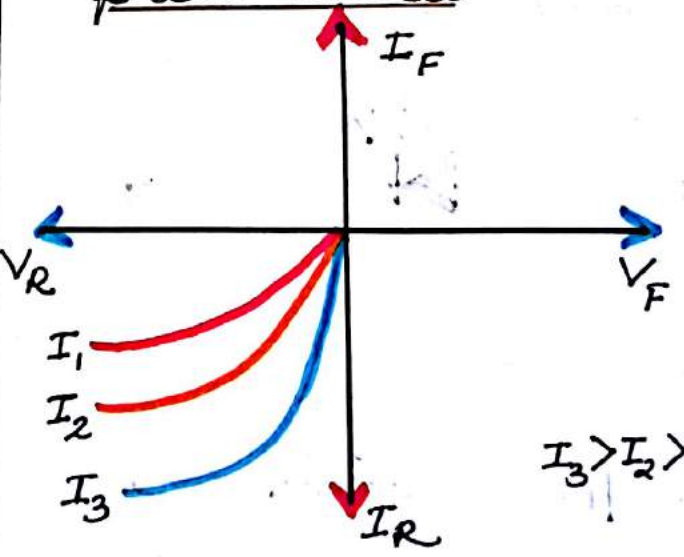
NB:- If input decreases due to fluctuation, current through zener diode and R_s decreases. Voltage drop accross R_s decreases without any change in voltage in zener diode

PHOTO DIODE



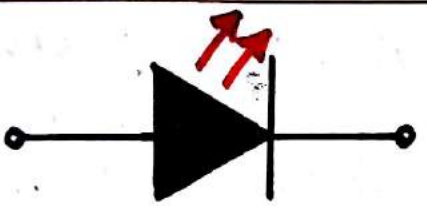
* Photo diode is an opto-electronic device
* It has a transparent window for the light to fall. It is operated in reverse bias region.
* photo diode is used to detect optical signal only if energy of light falling on it is greater than the energy gap ($E > E_g$) of the semiconductor.

* when light ray of energy ($E > E_g$, $E = h\nu$) fall on a transparent window of photo diode, electron-hole pairs are formed & then seperated.
* Due to electric field ele trons are collected on n-side and holes are collected on P-side resul ts in emf.
* when load resistance (R_L) is connected by re verse bias, photo current in μA flows throu gh the circuit.
* on Increasing the Int ensity of light photo current also Increases. photo current $\propto$ Intensity
* VI characteristics of photo diode

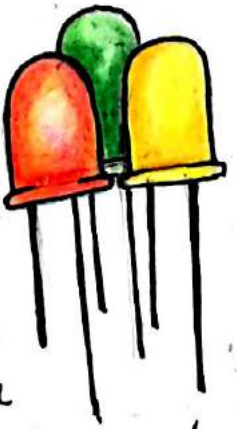


where I_1, I_2, I_3 are the intensities.

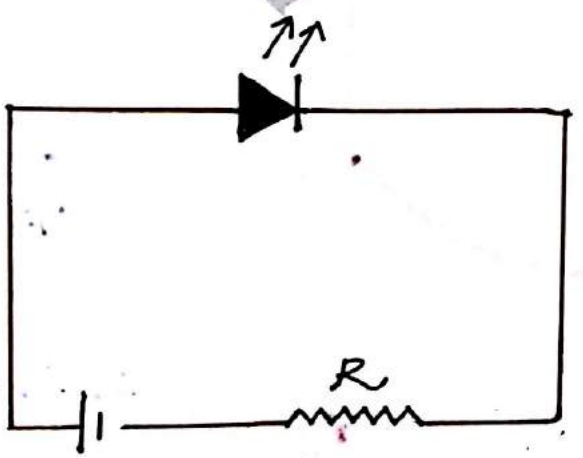
Light Emitting Diode [LED]



Symbol



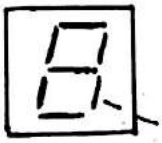
* It is a heavily doped p-n junction which under forward bias emits spontaneous radiation
* when forward biased e-h recombine near the junction and Energy is released in the form of photons ($E = h\nu = \frac{hc}{\lambda}$)
* As reverse break down voltage of LED is very low, care must be taken
* LED's can emit red, yellow, orange, green, blue light etc.
* GaAs – LED ($E_g \sim 1.9$ eV) used to make IR LED's



* A forward biased LED.

uses

1, Display in watches, calculators etc



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→ LED segment

2, Infra red LED's (IR LED's) are used in Bulgar-alarm systems

3, Indicator lamps.

4, Advanced display (AMOLED's, OLED's) and lighting systems.

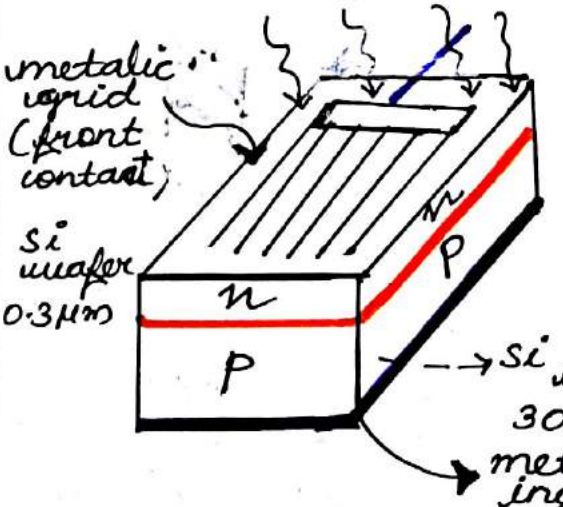
Advantages

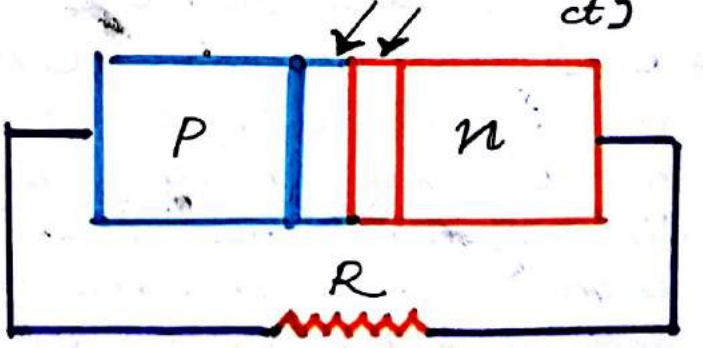
1, low operational voltage & less power

2, long life

3, Fast action & no warm up time required.

Solar Cell

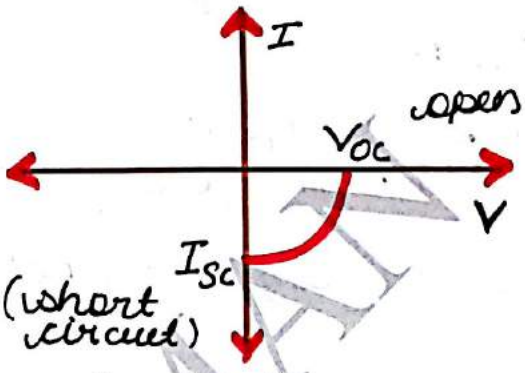




converts light energy into electrical energy.
eg; Si, Ge, selenium etc.
principle - same as photodiode [but no need to give external biasing]
→ A solar cell has a p-type semiconductor of thickness 300μm Si wafer with metal coating on one side called back contact.
→ It has n-type semiconductor of thickness 0.3μm Si wafer with a metallic grid called front contact.
→ when solar energy falls on solar cell three processes takes place.
(a) Generation of e's & holes.
(b) seperation of e's & holes.
(c) collection of e's & holes.
* Thus e's on n-side and holes on p-side collected due to potential difference in the depletion region.
* when an external load is connected a photo current I_L flows through the load.
note:- electrons reaching n side are collected by front contact & holes reaching p-side are collected by the back contact giving rise to photo voltage.

uses
1. power electronic devices in satellites and space vehicles
2. calculators.

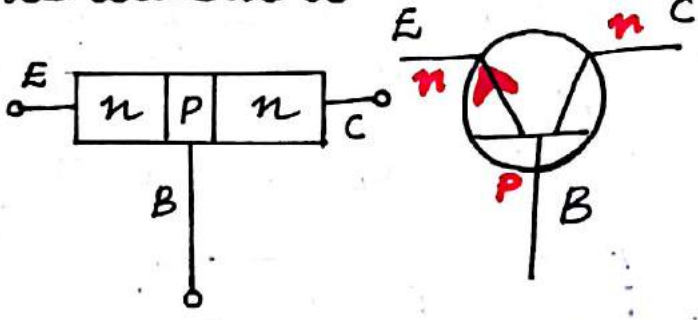
V-I characteristic



* It is in fourth quadrant because solar cell does not draw current but supplies the same to the load.

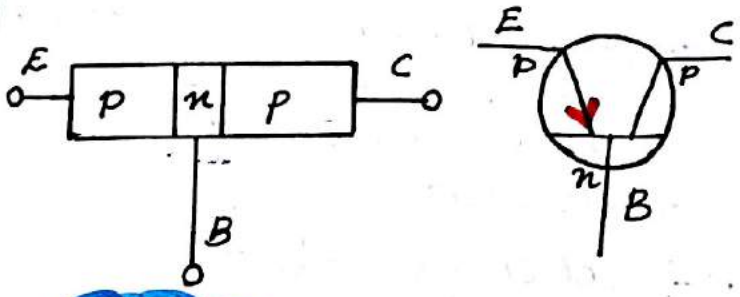
TRANSISTOR

A transistor has three doped regions forming two p-n junctions between them.
(a) n-p-n transistor.
p type transistor is sandwitched between two n type semiconductors



(b) p-n-p transistor
n-type semiconductor is sandwitched between 2 p type

semiconductors.



Emitter

* Heavily doped
* To emit majority carriers.
* physical size is moderate

Base

* lightly doped
* physically very thin

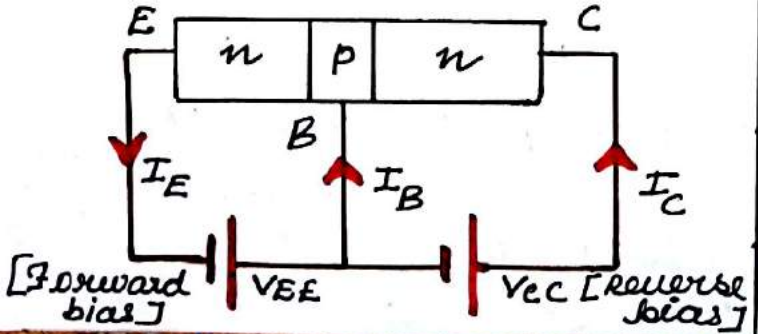
Collector

* moderately doped
* physically larger
* To collect majority carriers.

→ How to bias a Transistor?

1. Emitter - base junction should be forward biased to emit majority carriers.
2. collector-base junction should be reverse biased to collect the majority carriers.

→ Working of Transistor



* Emitter base junction should be always forward bias to emit majority carriers.
* collector base junction should be reverse biased to collect majority carriers.
* Majority carriers (e's in n region) are repelled by biasing voltage V_{EE} and injected to base region.
* In the base electrons are minority carriers, injected electrons from the emitter combines with holes in base and get neutralised [very small fraction] I_B
* The remaining majority carriers are collected by collector due to the reverse bias of common base junction
* According to Kirchoff's law

$$I_E = I_B + I_C$$

configurations of Transistor

1. common base configuration [CB]
2. common emitter configuration [CE]
3. common collector configuration [CC]

(1) common base configuration.

(a) Input resistance

$R_i = V_{EB}/I_E$

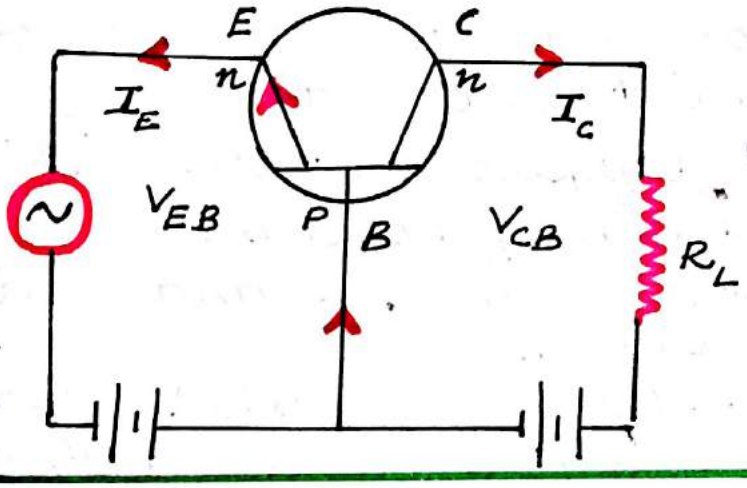
(b) output resistance

$R_o = V_{CB}/I_c$

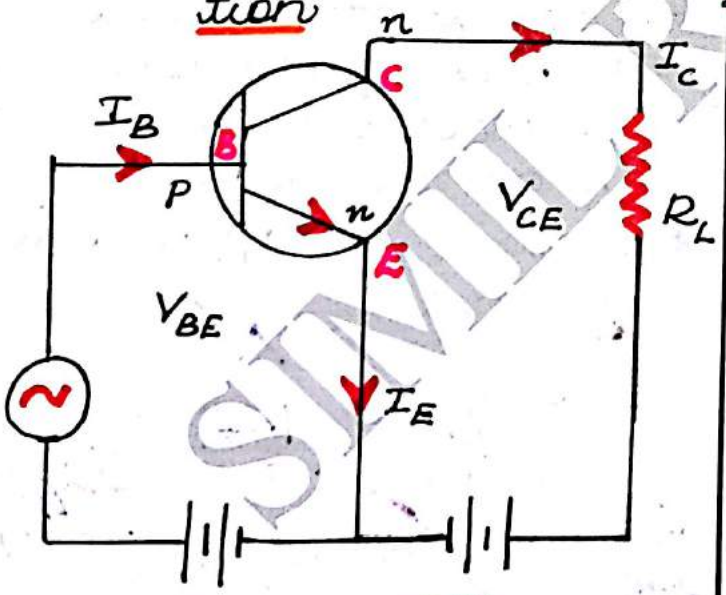
(c) current gain

$\alpha_{dc} = I_c/I_E$

$\alpha_{ac} = \Delta I_c/\Delta I_E$



2; Common emitter configuration



(a) $R_i = V_{BE}/I_B$

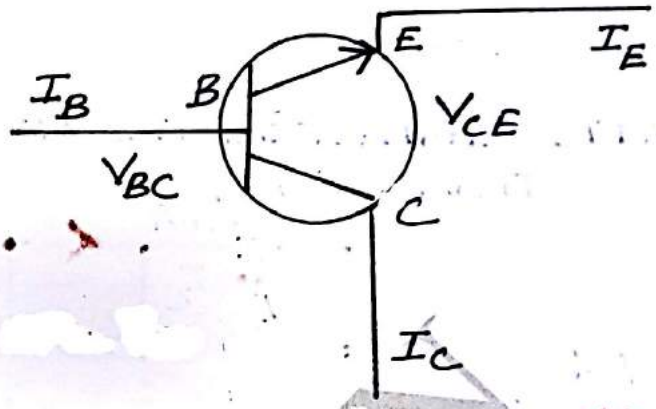
(b) $R_o = V_{CE}/I_c$

current gain

$\beta_{dc} = I_c/I_B$

$\beta_{ac} = \Delta I_c/\Delta I_B$

common collector configuration.



$R_i = \frac{V_{BC}}{I_B}$ $R_o = V_{CE}/I_c$

current gain

$\gamma_{dc} = I_E/I_B$

$\gamma_{ac} = \Delta I_E/\Delta I_B$

Relationship between α and β

$\alpha = \frac{I_c}{I_E}$, $\beta = \frac{I_c}{I_B}$

Kirchhoff's law

$I_E = I_B + I_c$ ... (1)

(1) $\div I_c$

$\frac{I_E}{I_c} = \frac{I_B}{I_c} + 1$

$\frac{1}{\alpha} = \frac{1}{\beta} + 1$

$\frac{1}{\beta} = \frac{1}{\alpha} - 1$

$\frac{1}{\alpha} = \frac{1+\beta}{\beta}$

$\alpha = \frac{\beta}{1+\beta}$

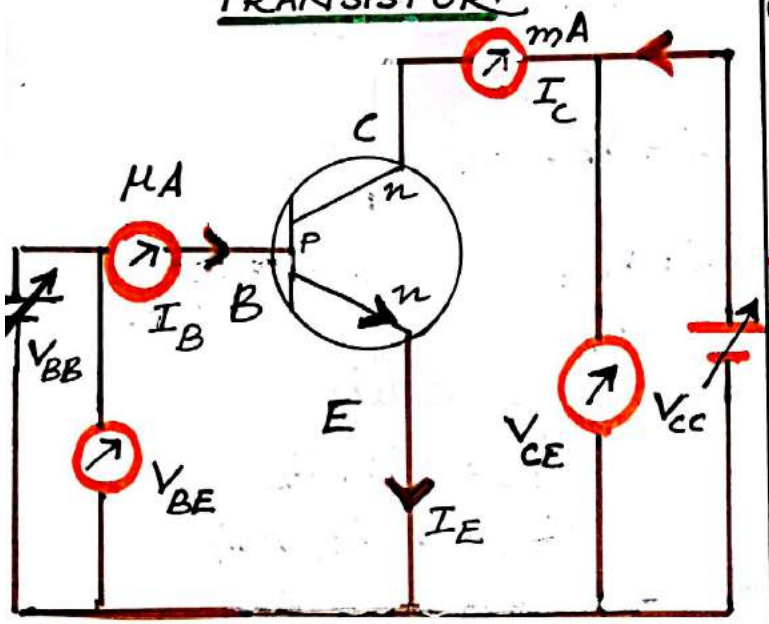
or

$\frac{1}{\beta} = \frac{1}{\alpha} - 1$

$$\frac{1}{\beta} = \frac{1-\alpha}{\alpha}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

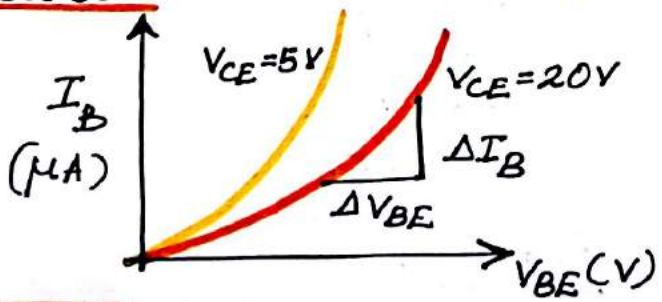
STATIC CHARACTERISTICS OF TRANSISTOR.



(a) Input characteristic

* Keep V_{CE} constant
* Increase V_{BE} and measure I_B.
* Plot a graph V_{BE} versus I_B – called input characteristic.
* To repeat the experiment, keep V_{CE} at some other constant value and again repeat the same.

→ Input characteristic curve

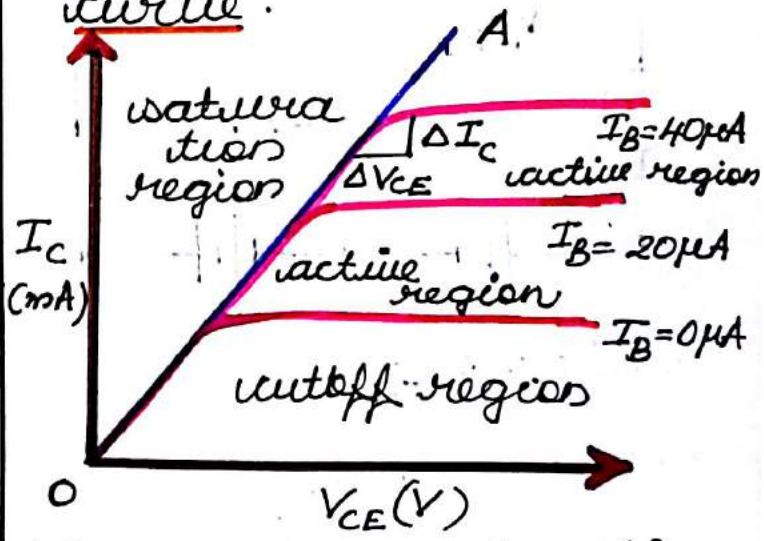


$$R_i = \left(\frac{\Delta V_{BE}}{\Delta I_B}\right)_{V_{CE}}$$

Input resistance is the ratio between small change in base emitter voltage to the small change in base current at constant collect er-emitter voltage.

(b) Output characteristic

* Keep I_B constant
* Increase V_{CE} and measure I_C
* Plot a graph V_{CE} versus I_C – called output characteristic.
* To repeat the experiment, keep I_B at some other constant value and repeat the same.
* output characteristic curve.



* OA – saturation line.

→ cut off region

Region below

I_B = 0μA

both input and output are reverse biased

→ saturation region

* Region left to OA - saturation line.
* Both Input and output are forward biased.

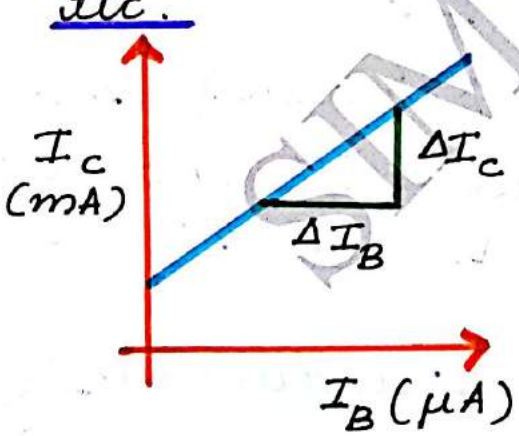
→ Active region

* Input forward biased and output reverse biased.
* Region above $I_B = 0\mu A$

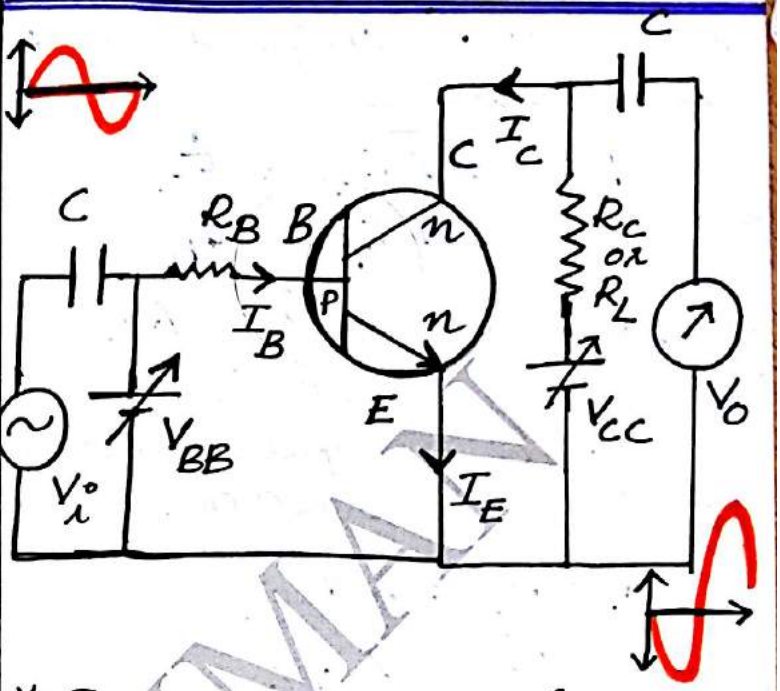
$$R_0 = \left(\frac{\Delta V_{CE}}{\Delta I_C}\right)_{I_B}$$

output resistance is the ratio between small change in collector emitter voltage and collector current.

(c) Transfer characteristic.



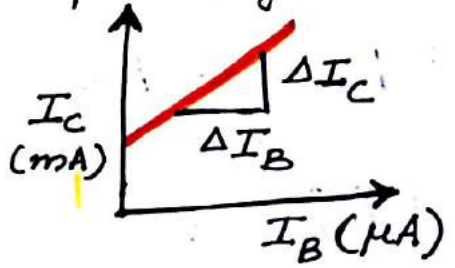
* Increase I_B and measure I_C
* Plot a graph I_B versus I_C
* current gain $\beta = \frac{\Delta I_C}{\Delta I_B}$



* Transistor used as amplifier in active region.
* C and C' - capacitors will not allow dc voltages for amplification
* V_{BB} and V_{CC} - dc voltages for biasing.

Amplification

For a small change in base current (ΔI_B), there is a great variation collector current (ΔI_C). It results in the amplification of input signal.



current gain (B)

It leads to gain

in current. [Ratio of change in collector current to change in base current.]

$$\beta_{ac} = \frac{\Delta I_C}{\Delta I_B} = \frac{i_c}{i_B}$$

(b) **Voltage gain (A_V)**

It is the ratio of output voltage to input voltage.

$$A_V = \frac{V_o}{V_i} = \frac{\Delta V_{CE}}{\Delta V_{BE}}$$

$$A_V = \frac{\Delta I_C R_C}{\Delta I_B R_B}$$

$R_B = R_i$, $R_C = R_L$, $\frac{\Delta I_C}{\Delta I_B} = \beta_{ac}$

$$A_V = \beta_{ac} \frac{R_L}{R_i}$$

$$A_V = -\beta_{ac} \frac{R_L}{R_i}$$

-ve sign indicates V_o is out of phase by 180° from V_i

(c) **Power gain (A_P)**

$$A_P = A_V \times \beta_{ac}$$

$$= \beta_{ac} \frac{R_L}{R_i} \beta_{ac}$$

$$A_P = \beta_{ac}^2 \frac{R_L}{R_i}$$

(d) **Reason for 180° phase difference between V_i and V_o**

$$V_{BB} = V_{BE} + I_B R_B$$

$$V_{CC} = V_{CE} + I_C R_C$$

V_{CE} is the output voltage

$$V_{CE} = V_{CC} - I_C R_C$$

$$V_o = V_{CC} - I_C R_C$$

(i) If input voltage (V_i) decreases input current (I_B) decreases, o/p current I_C decreases.

$I_C \downarrow$ & $V_o \uparrow$ (increases)

$\Rightarrow V_i \downarrow$ $V_o \uparrow$

(ii) If V_i increases $I_B \uparrow$

$I_C \uparrow$ $V_o \downarrow$

$\Rightarrow V_i \uparrow$ (increases) $V_o \downarrow$

∴ phase difference between V_o and V_i is 180°.

(e) **Transconductance (g_m)**

$$g_m = \frac{\Delta I_C}{\Delta V_{BE}} = \frac{\Delta I_C}{\Delta I_B R_i}$$

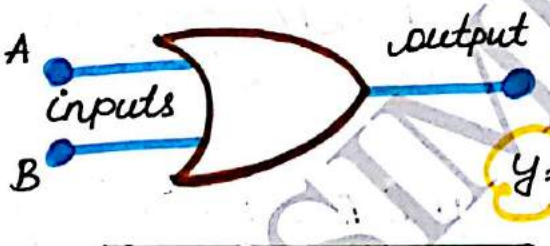
$$\therefore g_m = \frac{\beta_{ac}}{R_i}$$

LOGIC GATES

* The circuit which gives logical relationship between input and output.
* The algebra used in logic gates is boolean algebra.
* A digital circuit with one or more input signals but only one output signal is called a logic gate.

OR gate

An OR gate has two or more inputs with one output. The logic symbol and truth table are shown.



input		output
A	B	Y = A+B
0	0	0
0	1	1
1	0	1
1	1	1

→ Truth Table

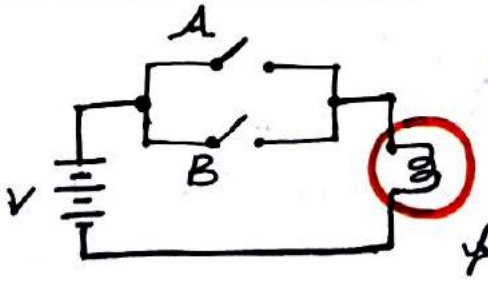
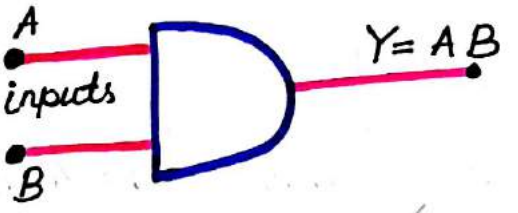


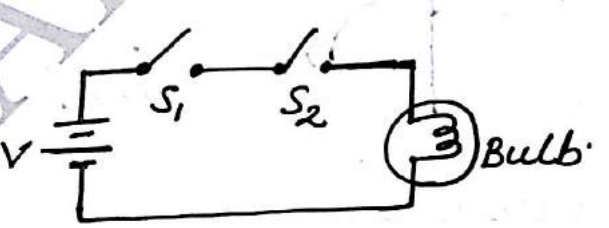
fig (i)

fig ii → If A & B closed bulb glows.

AND Gate

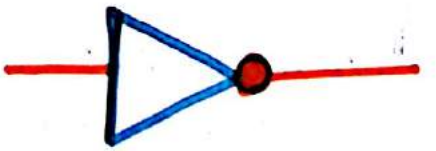


		output
A	B	Y = AB
0	0	0
0	1	0
1	0	0
1	1	1



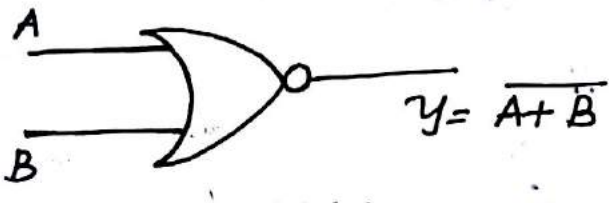
NOT gate

The NOT gate or inverter is the simplest of all logic gates. It has only one input and one output.



Input	output
A	Y
0	1
1	0

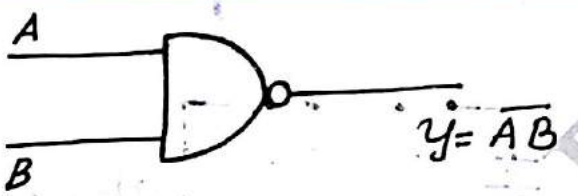
NOR gate



Truth table

A	B	A+B	$Y = \overline{A+B}$
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

NAND gate



Truth table

A	B	A·B	$\bar{y} = \overline{A \cdot B}$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

NAND & NOR gates are called universal gates because we can obtain all gates using NAND and NOR gates.

INTEGRATED CIRCUITS

The concept of fabricating an entire circuit on a small single block of a semiconductor is known as IC

* consisting of passive components — R, C
active components — diode, transistor.

Types of IC

(i) Monolithic IC :- Active and passive components are fabricated on a silicon wafer

(ii) Hybrid IC :- Active and passive components are fabricated on seperate silicon wafer.

* Analogue IC :- gives continuous variation of signal

* Digital IC :- not continuous only '0' or '1'.

Different levels of IC

(i) small scale Integration (SSI)
no of gates < 10

(ii) Medium scale Integration (MSI)
No of gates between 10 and 100.

(iii) Large scale Integration (LSI)
logic gates between 100 – 10,000

(iv) Very large scale Integration (VLSI)
logic gates more than 10,000
eg. micro-processor chips.

(v) Ultra large scale Integration (ULSI)
gates $> 10^6$

Advantages of IC

(i) Low cost
(ii) high reliability
(iii) shock-proof
(iv) require low power

Disadvantages of IC

(i) Transformers, inductors, capacitors of high value cannot be fabricated.
(ii) If any part of IC is out of order entire IC needs to be replaced.
(iii) cannot be operated at high power.